Mercury FID Electronics Circuit Description
Revision: 2
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1. Applicability

This document applies to Mercury FID schematic 03-925024-00, Revision C1.

2. Power supplies and grounds

There are four grounds serving the FID electronics circuitry. Ground 1 is the return for the +5V digital supply. It is connected directly to Ground 4, the unregulated +24V return, at the card edge connector on the Mother board. The analog return is Ground 2, which provides a low-noise return for the ±15V and +5.25V supplies. Ground 3 is the reference for analog signal distribution, which carries almost no DC current. All of the grounds must be tied together externally for the board to function properly.

Three RC filters remove noise from the analog power supplies. These consist of R24 with C13, R23 with C12, and R22 with C11.

3. Digital circuits

U7 decodes bus address information to access latch U6 and buffer U5. The latch holds all of the digital control signals for the board, while the buffer transmits the board identification number and serial data from EEPROM U8 to the bus. R25 allows the inputs of U5 to be pulled high for test, while remaining low in normal operation.

The EEPROM is a 1024-bit device which is used to store calibration data. Software has full control over the serial interface, consisting of the chip select, shift clock, and data inputs (pins 1 - 3, respectively), and must reassemble the stored data from the serial output stream coming from pin 4. When the EEPROM is not selected, its output is high impedance. R26 provides a positive level to CMOS buffer U5 in this case.

4. Input log amplifier of square-root electrometer

The electrometer is a multi-stage circuit which produces an output voltage which is proportional to the square-root of the input current. This is accomplished by three amplifier stages, AR1 (dual) and AR2, having logarithmic and exponential responses. The nonlinear responses are generated by the fundamental characteristic of bipolar transistors, which is represented in the following equations:

$v_{be} = (nkT/q) \log(I_c/I_{sat} + 1)$ or $I_c = I_{sat} (e^{(qv_{be}/nkT)} - 1)$,

where v_{be} = base-emitter voltage (volts)
n = emission coefficient (near 1.00)
k = Boltzmann's constant (1.38E-23 Joule/K)
T = Temperature (Kelvins)
q = electron charge (1.6E-19 coulomb)
I_c = collector current
I_{sat} = saturation current
e = base of natural logarithms

Input amplifier AR2 has an extremely high input impedance, with a bias current of only about 40fA (40 x 10^{-15}A). All of the input current from J1 must therefore flow into the collector of Q1 (pin 8). Negative feedback from the output of AR2 adjusts the base-emitter voltage of Q1 until precisely this current flows into the collector. The output voltage from this stage, which is taken from the emitter of Q1 (pin 6), is therefore $v_{eb1} = - (nkT/q) \log(I_{in}/I_{sat} + 1)$.

The output voltage must be negative in order to forward-bias the base-emitter junction of Q1. However, the negative power supply for AR2 is ground, so its output cannot go below ground. R4 and R5 provide about 700mV of negative offset, allowing the output of AR2 to remain positive, while Q1 is turned on. R5 also stabilizes the loop gain at input currents near full scale (1μA), where the impedance looking into the emitter of Q1 has dropped to 26k.

Since the non-inverting input of AR2 is grounded, the inverting input remains at ground also, keeping the collector of Q1 at ground. This holds the collector-base voltage at zero, which is a necessary condition for the equations above to apply. The input connection at J1 also remains near ground at low input currents, minimizing noise due to variations in input capacitance. R1 limits input current if an excessive voltage is applied to the input, but it also allows the input voltage to rise slightly at the higher input currents. R2, which isolates the amplifier input from the input cable capacitance for loop stability, has almost no DC voltage drop across it, since only the bias current of AR2 flows through it. C3 also enhances loop stability, and reduces high-frequency noise.

Because of the high impedance levels, this entire circuit must be shielded to work properly at all but the highest input currents. It is also easily upset by test probes even when shields are in place. In any case, the exact output voltage to be expected at a particular input current is unknown, since the saturation current of the input log transistor is unknown. All that can be predicted is that the output voltage will increase (in a negative direction) by about 26mV when the input current is doubled, or by 60mV when the input current is raised by ten times, regardless of the specific current levels.

5. Reference current log amplifier

The saturation currents of the individual transistors vary from one unit to the next, and also change rapidly with temperature, doubling with each 10°C rise. In order to maintain stable and predictable calibration, each transistor used in the anti-log stage must be balanced by a matching transistor in a log stage. The anti-log stage uses two transistors, as will be described below, so a second log amplifier is needed for compensation purposes. This stage consists of one section each of AR1 (pins 1-3) and Q2 (pins 6-8), and is very similar to the input log amplifier.

The sum of the two emitter-base voltages of the log transistors is produced directly by connecting them in series. The emitter of Q1 (pin 6) is connected to the base of the Q2 (pin 7), and the output v_{sum} is taken from the emitter of Q2 (pin 6). The collector of Q2 (pin 6) is connected to the inverting input of AR1 (pin 2), which is held at the same voltage as the noninverting input (pin 3). By connecting the base of Q2 (pin 7) to the noninverting input, the collector-base voltage is forced to be zero. This causes the inverting input to follow the output voltage of AR2 (pin 1). As this voltage varies by a few hundred millivolts over the full range of the input current, the reference current (I_{ref}) through R6 varies between 23 and 24 microamps. The emitter-base voltage of Q2 is thus $v_{eb2} = - (nkT/q) \log(I_{ref}/I_{sat} + 1)$, and the net voltage at the emitter of Q2 is

$$v_{sum} = - (nkT/q) \log(I_{in}/I_{sat} + 1) - (nkT/q) \log(I_{ref}/I_{sat} + 1)$$

$$= - (nkT/q) \log ((I_{in}/I_{sat} + 1)(I_{ref}/I_{sat} + 1)).$$

AR1 is powered from the ±15V power supplies, which could cause avalanche breakdown of the emitter-base junction of Q2, if the amplifier output ever approached the positive supply voltage. While this never occurs in normal operation, even a momentary breakdown can cause a permanent increase in saturation current. CR1 prevents the emitter voltage from rising to a destructive level during testing or other transient fault conditions.

6. Anti-log amplifier

The logarithmically compressed voltage v_{sum} is applied to an anti-log (or exponential) amplifier stage which utilizes the other halves of matched dual transistors Q1 and Q2. Since the anti-log transistors are connected in series, both collector currents are essentially equal. If we assume that all of the transistors are at the same temperature T and have the same saturation current I_{sat}, the base-emitter voltage of each of the anti-log transistors will be half the value of v_{sum}. Their collector currents must then be $I_c = I_{sat} (e^{-(qv_{sum}/2nkT)} - 1)$ from the equation in section 4. Substituting the expression for v_{sum} above, we have

$$I_c = I_{sat}\,(e^{(1/2)\log((Iin/Isat + 1)(Iref/Isat + 1))} - 1)$$

$$= I_{sat}\,(\mathrm{sqrt}((Iin/Isat + 1)(Iref/Isat + 1)) - 1)$$

$$= \mathrm{sqrt}((I_{in} + I_{sat})(I_{ref} + I_{sat})) - I_{sat}$$

$$= \mathrm{sqrt}((I_{in} + I_{sat})(I_{ref})) - I_{sat} \qquad (\text{since } I_{ref} > 10^9 \text{ x Isat})$$

Amplifier AR1 holds the collector of Q1 (pin 1) at ground potential and forces the collector current to flow through R3. The final output voltage at P1-1 is then

$$v_{out} = 2.05 \text{ x } 10^6 \text{ x } \mathrm{sqrt}((I_{in} + I_{sat})(I_{ref})) + v_{os},$$

where v_{os} is the sum of the input offset voltage of AR1 and all of the current-related voltage errors. Putting in the nominal value of 25 microamps for I_{ref} gives the following approximate formula for the output voltage:

$$v_{out} = 10^4 \text{ x } \mathrm{sqrt}(I_{in} + I_{sat}) + v_{os}.$$

This formula will not be accurate if the temperatures of all of the transistors are not equal. The two halves of each dual transistor are always at the same temperature, since they are fabricated on a single silicon die. Q1 and Q2 track each other in temperature only by being in close proximity in an isolated environment, however, and any thermal disturbance will cause the output of the electrometer to drift. Simply touching one of the transistors can cause a minute or two of drift, and the output may not stabilize for 5 or 10 minutes after soldering in the vicinity of the transistors.

The time constant of the amplifier is set to 45ms by C1, and C2 eliminates high-frequency noise from digital sources. R8 and C10 prevent glitches from the ADC multiplexer (on the main system board), which reads the output voltage of the electrometer, from disturbing the amplifier output. Such glitches can couple through C1 and the capacitance between the collectors of the two halves of Q1 to disturb the sensitive input node, resulting in a much longer settling time than would be expected.

7. Electrometer diagnostic features

In order to determine the input current from the output voltage, the value of v_{os} in the equation in the preceding paragraph must be determined. This is done during operation by closing the switch section of U1 (pins 1-3) which is connected to the output of the reference log amplifier. Current through the anti-log transistors is thus cut off, leaving the output voltage at P1-1 equal to v_{os}.

Though it is not immediately obvious from the equations presented here, closing the switch section of U1 (pins 14-16) which is connected to the output of the input log amplifier results in an output voltage at P1-1 which corresponds to an input current equal

to the saturation current of Q1. This measurement is used for diagnostic purposes only. Both of the diagnostic switch sections of U1 are left open in normal operation.

Because the input stage of the electrometer has a logarithmic response, its behavior becomes unpredictable as the input current approaches zero. All of the voltages applied to the circuit are above ground potential, so leakage currents should never cause the input to reverse in polarity and saturate the output positively. However, the response time of the circuit is inversely proportional to the current level, becoming very slow at currents below a few hundred femtoamps. For this reason, it is impractical to test the noise and drift of the electrometer by "capping off" the input with no input current.

To test the electrometer when no external picoamp source is available, an input current source in the picoampere range has been provided. This source relies upon the fact that the current through a capacitor is equal to the product of the capacitance and the rate of change of the voltage across the capacitor. C4 (10pF) is connected to the electrometer input, which remains near ground potential. Applying a positive sawtooth waveform to the other end of C4 should thus produce a steady input current, with negative spikes on the negative transitions of the sawtooth voltage. This waveform (modified somewhat to optimize the recovery of the electrometer from the negative spikes) is generated by an external DAC and applied to C4 through a filter consisting of R10 and C9. The filter removes noise from the external input, while slowing the transitions somewhat. In normal operation, transistor Q3 is turned on by writing a logic 1 to U6-12, shorting C4 to ground. Voltage variations at P1-10 will then not create an undesired current at the electrometer input.

8. High voltage power supply

The high voltage power supply provides a stable source of 190VDC at low current. It consists of a linear regulator operating from the +24V supply, an unregulated flyback converter, and a zener diode regulator.

VR1 pre-regulates the power supplied to the flyback converter, thereby stabilizing the current which is supplied by the converter to the zener diode. It also powers U2 and U3, which sets the drive voltage for the gates of Q4-Q6 at 15V.

U4, a TL494, is a controller for pulse-width-modulated switching power supplies. In this application, however, it is used only to provide fixed, 45% duty cycle pulses. The internal error amplifiers are set to their maximum duty cycle condition by tying their noninverting inputs (pins 1 and 16) to ground, and connecting their inverting inputs (pins 2 and 15) to the 5-volt VREF (pin 14). Maximum duty cycle (45%) is achieved by turning off analog switch U1 (pins 6-7), so that R14 pulls the dead time input (pin 4) down to ground. The converter is turned off by closing the switch, pulling up the dead time pin to 5 volts and setting 100% dead time (0% duty cycle). R15 and C19 set the operating frequency to 50kHz.

The outputs of U4 are uncommitted transistors, which conduct alternately without overlap. Their emitters are tied to ground (pins 9 and 10), and their collectors are pulled up to 15 volts through R12 and R13. U3 (pins 1-3) inverts the negative-going pulses from one of the outputs, and two sections of U2 provide provide a high-current drive to switch the large gate capacitance of Q4 quickly. Q4 is on for about 10μs for each pulse, placing 15 volts across 1.2mH inductor L1. The current in L1 ramps up to about 100mA while Q6 is conducting. When Q6 turns off, the voltage on the drain of Q4 (pin 3) rises rapidly, turning on CR2. The energy which was stored in the inductor is transferred into C14. The voltage across C14 stabilizes at the voltage which lets the energy flow out of it at the same rate as it flows in. This occurs at about 210V, with about 500μA flowing through R17 and VR2. R18 and R19 limit the current from the supply to a safe value in case of operator contact, while C15 and C18 reduce noise pickup on this high-impedance line.

Resistors R20 and R21 divide the high voltage by 202 for measurement by the system ADC. The current drawn by this divider drops the nominal voltage at J2-1 to 191VDC. If this point is measured with a typical meter having a 10M input resistance, the nominal reading falls to 173V.

9. Igniter power supply

The igniter power converter supplies 6.4Vp-p (unregulated) square waves for the FID flame igniter. It is driven from both outputs of U4, so the high voltage must be turned on in order to enable the igniter supply. The igniter supply is then turned on by turning on U1 (pins 9-11). U3 and U2 invert and buffer the push-pull outputs to drive transistors Q5 and Q6, as in the high voltage supply. If U1 (pins 9-11) is turned off, R11 pulls U3-6 and U3-9 high, holding both transistors off by grounding their gates. Transformer T1 steps down the 24V square waves at pins 1 and 3 to 6.4Vp-p across pins 4 and 6.

Stray capacitance from the primary of T1 to its secondary circuit couples 50kHz square wave currents into Ground 3. C20 provides a direct path to return these currents to Ground 4.

10. Log of revisions and file identification

Rev. Draft 1 7/6/94

Rev. 1 7/13/94 Minor corrections and clarifications.

Rev. 2 4/7/95 Main changes:

Updated reference designators to match renumbered Rev. C1 assembly.
Described new circuit for high voltage power supply (hardware change in Rev. C1).

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